REMARKS

Claims 1, 2, 7, 8 and 18 have been amended and claims 10 and 11 have been cancelled without prejudice. Claims 1 to 4, 7 to 9 and 18 to 24 remain active in this application.

The attached drawings are proposed to be amended as required without the addition of new matter as shown in red. Approval is respectfully requested.

The claims have been amended to remove the objections thereto.

Claims 7 to 9 and 18 to 24 were rejected under 35 U.S.C. 112, first paragraph, as being based upon a non-enabling disclosure. The claims have been amended to overcome the rejection since the disclosure is clearly enabling.

Claims 1 to 4, 10, 11 and 18 to 24 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The claims have been amended, as required, to overcome this rejection.

Claims 1, 3, 18 to 21, 23 and 24 were rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi (U.S. 5,087,585). The rejection is respectfully traversed.

Claim 1 requires, among other steps, forming an electrically insulating layer having a pair of opposed outer faces, one of the outer faces disposed on the surface one of the substrate or the device wafer, the electrically insulating layer having an electrical interconnect structure disposed therewithin, a portion of the interconnect structure extending substantially to the one of the outer faces of the electrically insulating structure and then bonding the other of the outer faces of the electrically insulating layer to the surface of the other of the substrate or device wafer. No such steps in the combination as claimed are taught or suggested by Hayashi.

Claim 3 depends from claim 1 and therefore defines over Hayashi for at least the reason provided above as to claim 1.

In addition, claim 3 further limits claim 1 by requiring that at least one of the device layer and the substrate include a bond region, the interconnect structure contacting the bond region. insulating layer sufficient to break down said portion of said electrically insulating layer while maintaining the integrity of the remainder of said SOI structure

Claim 18 requires, among other steps, after providing a device layer having at least one of active or passive elements on a surface thereof and providing a substrate having at least one of active or passive elements on a surface thereof, providing a dielectric bonded to one of the device layer and the substrate having an interconnect disposed therein and extending to at least one surface thereof and then bonding the dielectric to the other of the device layer and the substrate to form an interface with the one of said device layer and the substrate and form an electrically conductive path across the interface to the interconnect. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claims 19 to 21, 23 and 24 depend from claim 18 and therefore define patentably over Hayashi for at least the reason presented above with reference to claim 18.

In addition, claim 19 further limits claim 18 by requiring that the electrically conductive path contacts the other of the device layer and the substrate. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claims 20 and 21 further limit claims 18 and 19 by requiring that the electrically conductive path be an extension of said device layer. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claim 23 further limits claim 18 by requiring that the substrate be a semiconductor substrate. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claim 24 further limits claim 18 by requiring that the substrate comprise a semiconductor substrate and a dielectric. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claim 7 was rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi (U.S. 5,573,972). The rejection is respectfully traversed.

Claim 7 requires, among other steps, in an SOI structure having a device layer having at least one of active or passive elements on a surface thereof, a substrate having at least one of active or passive elements on a surface thereof and an electrically insulating layer having an interconnect structure disposed therein and extending to a surface thereof, the interconnect structure separating a portion of the device layer from said substrate, the steps of forming a substantially planar surface comprising areas of one of the device layer and the substrate and areas of the electrically insulating layer and then bonding the surface to the other of the substrate wafer and device layer. Note that Kobayashi has no electrically insulating layer having an interconnect structure which provides the claimed interconnect function is the electrically insulating layer bonded to one of the device layer or substrate after being affixed to the other of these elements in the manner claimed.

Claims 1 to 4 and 18 to 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi in view of Applicant's admitted prior art. The rejection is respectfully traversed.

The arguments presented above as to Hayashi is repeated since Applicant's admitted prior art does not overcome the demonstrated deficiencies in Hayashi. Claim 2, 4 and 22 are further patentable over the applied references since they depend from one of claim 1 or 18 as discussed above.

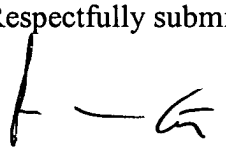
Claim 2 further limits claim 1 by requiring the step of applying a voltage across a portion of the electrically insulating layer sufficient to break down the portion of the electrically insulating layer while maintaining the integrity of the remainder of SOI structure. No such combination is taught or suggested by Hayashi, the admitted prior art or any proper combination thereof.

Claim 4 further limits claim 2 by requiring that at least one of the device layer and the substrate include a bond region, the interconnect structure contacting the bond region through the portion of the electrically insulating layer. No such combination is taught or suggested by Hayashi, the admitted prior art or any proper combination thereof.

Claim 22 further limits claim 18 by requiring that the step of forming an electrically conductive path across the interface to the interconnect be formed by breakdown of the dielectric. No such combination is taught or suggested by Hayashi, the admitted prior art or any proper combination thereof.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



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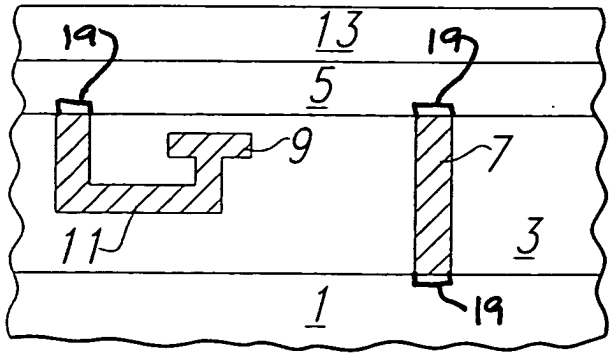

Fig.1

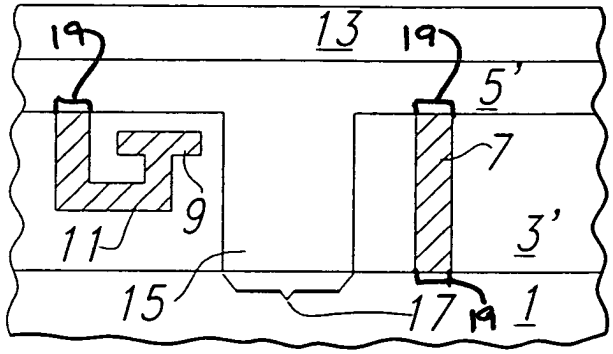

Fig.2

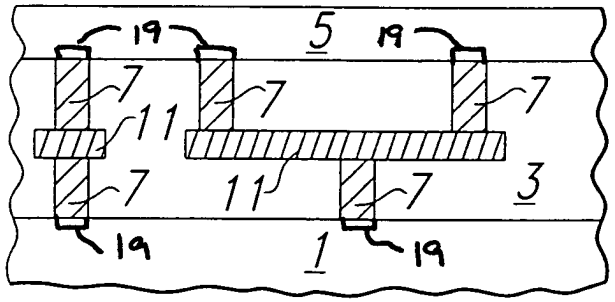

Fig.3

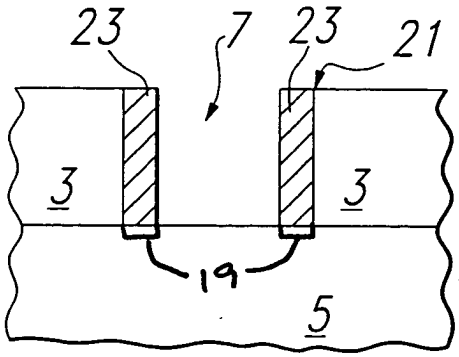

Fig.4

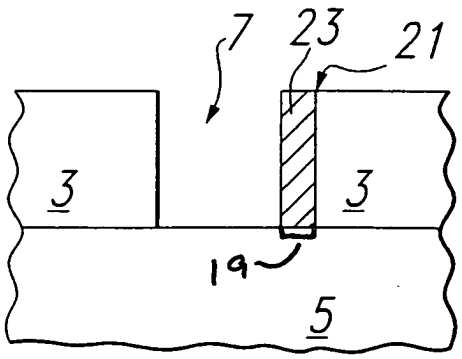

Fig.5

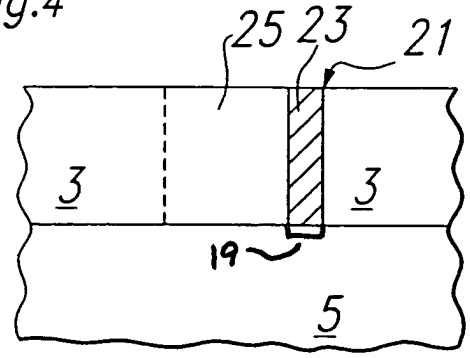

Fig.6